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CLOCK AND DATA RECOVERY SYSTEM FOR A WIDE RANGE OF BIT RATES

Abstract

A clock recovery system (10) for recovering an input data signal (14) clock. A rate detector (20) detects the input data signal bit rate and provides range signals (30a-c) specifying progressive ranges encompassing the bit rate. A frequency detector (22) provides a frequency error signal (32) based on frequency difference between the input data signal and a recovered clock signal (16). A phase detector (24) provides a phase error signal (34) based on the input data and recovered clock signals. A filter-controller (26) provides an oscillator driving signal (36) based on the range, frequency error, and phase error signals. An oscillator-divider (28) then provides the recovered clock signal based on the oscillator driving signal and at least some of the range signals. The phase detector, filter-controller, and oscillator-divider collectively thus form a phase locked loop. Optionally, the clock recovery system (10) may also provide a recovered data signal (18).